Docket No.: P2001,0300

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By:____________________ Date: January 22, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	Karl Mautz, et al.
Filed	:	October 27, 2003
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Customer No.:		24131

CLAIM FOR PRIORITY

Mail Stop: Missing Parts
Hon. Commissioner for Patents,
Alexandria, VA 22313-1450
Sir:

Claim is hereby made for a right of priority under Title 35, U.S. Code, Section 119, based upon the European Patent Application 011 10 455.1 filed April 27, 2001.

A certified copy of the above-mentioned foreign patent application is being submitted herewith.

Respectfully submitted,

GREGORY L. MAYBACK
REG. NO. 40,716

Date: January 22, 2004

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

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Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

01110455.1

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 01110455.1
Demande no:

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Anmelder/Applicant(s)/Demandeur(s):

Infineon Technologies SC300 GmbH & Co. KG
Königsbrücker Strasse 180
01099 Dresden
ALLEMAGNE
Infineon Technologies AG
St.-Martin-Strasse 53
81669 München
ALLEMAGNE
MOTOROLA, INC.
1303 East Algonquin Road
Schaumburg, IL 60196
ETATS-UNIS D'AMERIQUE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

M thod for adjusting processing parameters of at least one plate-like object in a processing tool

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Description

Method for adjusting processing parameters of at least one plate-like object in a processing tool

The present invention relates to a method for adjusting processing parameters of at least one plate-like object in a processing tool, said plate-like object being to experience at least one preceding processing step performed each by one processing device out of at least one set of processing devices, the adjustment in said processing tool being controlled by a control unit.

In semiconductor device or flat panel display, etc., manufacturing, minimum structure sizes are intended to be shrinked continuously in order to achieve high densities of patterns and structures in integrated devices.

Currently, lithography for structuring such patterns becomes increasingly challenging when extending to minimum structure sizes equal to or lower than 0.25 µm technologies. Strong requirements concerning critical dimension, overlay or alignment, etc., are to be fulfilled.

While limitations on minimum structure sizes can easily be investigated and derived from the lithography part of the semiconductor device manufacturing sequence of steps, such challenging limitations may also be inferred from other semiconductor device processing steps, in particular those preceding the lithography step. For example, in the case of semiconductor wafers, the step of chemical-mechanical polishing (CMP) is known to affect the structure of alignment marks either by obscuration of such marks or by producing inclined and offset, i. e. shifted, alignment profiles. Therefore, the abrading effect directly influences the alignment step prior to exposing the following resist layer.

Thus, since previous processing becomes increasingly important for the current step adjustment, methods have evolved to statistically increase the yield for the production of semiconductor devices. As shown in figure 1 for the example of manufacturing semiconductor wafers combined into lots, semiconductor wafers are provided to a processing tool, i. e. the lithography tool in this example, and are exposed and processed with a set of processing parameters such as alignment shifts and scales, exposure dose, or focus channel. The outcome of this process is controlled in an overlay tool which provides a feedback of the process quality to the lithography tool or its control unit, respectively. If the metrology results fail some specification, a new lithography run is done with new test wafers. To accomplish this, the metrology parameters like overlay, critical dimension, etc., are recalculated or reinterpreted by the control unit in terms of e.g. exposure parameter adjustments. The adjustments performed on the test wafers are then verified to be successful one more time using said overlay tool. Using this feedback cycle, production wafers eventually pass the metrology measurement in order to be further processed.

The measurement results and the process parameter settings are typically stored in a database for providing a calculation of those optimal parameter settings, which provide the highest yield of wafers.

This method, although providing a closed-loop control circuit, unfortunately comes together with several disadvantages. Time is spent by processing a number of test wafers in order to retrieve a production wafer, lithography tool capacity is reduced, test wafer material is consumed non-productively, and the time to produce a wafer is prolonged. In particular, the scatter in overlay measurement data of wafers in a lot statistically is still considerably resulting in a reduced yield.

It is therefore a primary objective of the present invention to reduce the amount of rework in manufacturing plate-like objects, e.g. semiconductor devices or flat panel displays, thereby improving the quality, and saving time and costs to produce a plate-like object.

The objective is solved by a method for adjusting processing parameters of at least one plate-like object in a processing tool, said plate-like object being to experience at least one preceding processing step performed each by one processing device out of at least one set of processing devices, the adjustment in said processing tool being controlled by a control unit, comprising the steps of providing a plate-like object to said processing device, processing said plate-like object, generating a token associated with said plate-like object, representing the processing device that has been used for the preceding processing step, transferring said token to said control unit, transferring said plate-like object to said processing tool, adjusting the process parameters of said processing tool using said control unit in dependence of the processing device being associated with said token, performing the process step on said plate-like object in said processing tool using the adjusted process parameters.

The term of plate-like object used in this document refers to devices comprising a substrate being to receive a structure on its surface in a sequence of processing steps involving critical variables (i.e. processing parameters), in particular semiconductor wafers, masks or reticles, compact discs, or flat panel displays. The following description of the invention concentrates on the case of semiconductor devices, but is also valid for other embodiments of plate-like objects as stated above.

The term processing tool refers to the manufacturing apparatus or arrangement, where according to the present method the processing parameters are to be adjusted. Processing device

refers to the apparatus or arrangement, which performed the preceding step in the sequence of steps for manufacturing the plate-like object. A step is defined as a physical or chemical process applied to the plate-like object, which changes a physical or chemical characteristic on or in it.

It is found that the statistical scatter in the overlay, critical dimension, layer thickness and other metrology data resulting from poorly chosen processing parameters in e. g. the lithography tool or other processing tools has one of its origins in the variation within groups of similar processing devices, which perform preceding processing steps prior to the processing tool under consideration. The differing processing conditions inside these devices generally vary from processing device supplier to supplier, but even vary within groups of processing devices of the same type.

Because e. g. the variations between the processing devices depend on conditions inferred most probably from the time of their construction, or system maintenance setups, these variations are reflected by parameter offsets that are constant for a time.

According to the method of the present invention, the semiconductor devices, e. g. wafers, which are commonly distributed over a set of processing devices performing the same tasks preceding the step currently under consideration, are each supplied with a token. The token consists of at least a pair of data which is the wafer identification and the processing device that has been used in the preceding step. The wafer identification is necessary in order to regain the information for the current process step under consideration of which processing device has been used in the preceding step. Typically, an identification is not physically marked on the semiconductor device or wafer surface. Rather, the name of the device carrier, which is used to transport devices through the fab, and the slot number enable a re-

identification of an individual wafer. Therefore, the tokens considered in the present method are preferably embodied as data signals exchanged between local hosts of the processing tools or devices via a fabrication-wide CIM-system.

Another possibility would be to supply the corresponding information put into tokens with the device carrier box, which can be read out locally at the processing tool under consideration.

It is also possible to regroup or reorder the semiconductor devices process in a preceding step according to the processing device used. By the slot number of the corresponding device in the device carrier, it is then known which processing device had been active to process the corresponding semiconductor device or wafer inside said slot. In this case, the slot number gives the wafer identification and a corresponding token can be generated.

A main advantage of the present invention is, that the processing parameters of the corresponding processing tool being under investigation can be adjusted for compensating the individual variations of said processing devices which affect characteristics of the semiconductor devices which are used to perform the current processing step. In the example of chemical-mechanical polishing of semiconductor wafers in a preceding step, an alignment mark that is constantly offset in one of the CMP-apparatus, by identification of the semiconductor wafer the token is analysed to give the identification of the processing device of the preceding CMP-step, and a control unit controlling the current lithographic processing tool can apply a compensating adjustment of the corresponding alignment parameters, if the constant offset of the CMP-apparatus is known.

Preferably, these data are stored in a database connected to the control unit. This adjustment advantageously leads to a

reduction of statistical scatter of metrology measurements of samples of semiconductor wafers or other devices such as flat panel displays. Moreover, since these variation effects can be compensated, tedious system maintenance of, e. g., the CMP-apparatus in order to eliminate the error or offset is now obsolete.

Therefore, the semiconductor device processing yield is advantageously increased and the waste of processing test wafers can effectively be reduced.

In single-wafer-tracking, or single-device-tracking, respectively, each wafer is processed with its own token. Since each token may reflect differing processing being used in a preceding step for the current wafer, the processing tool, e. g. the lithography tool, can have different adjustments of processing parameters from wafer to wafer. Because the token may be forwarded automatically and the control unit can analyse the token immediately, no operator efforts are necessary to control the processing tool adjustment for individual wafers or other semiconductor devices.

In a further aspect, the processing devices of the preceding step are considered to be at least one of chemical-mechanical polishing (CMP), etching or chemical vapour disposition (CVD).

Also, the processing tool in the case of semiconductor devices being wafers, needs not to be restricted to lithography tools. For example, it can be an etching tool while the preceding step preparing the etching is a developing step performed in a lithography cluster, etc.

Two further aspects consider different mechanisms of feeding quality measurements results to the control unit that needs to know how to adjust a processing parameter for a semiconductor device with a known preceding processing device due to

the token. In both aspects, the quality measurements are taken by metrology tools. In the first aspect, a corresponding metrology step is performed after the preceding processing step in a processing device but prior to the current processing step under consideration to be performed by the processing tool, e. g. an etching tool preceded by a developing step. An individual processing device parameter offset can be recognized by the metrology tool and the result for the corresponding semiconductor device, or wafer, be feed-forwarded to the control unit. The control unit receives the token of the wafer, identifies the processing device that has been used, and compares the measurement results with targets. This comparison then is converted into a new processing parameter adjustment for the wafer.

The control unit also may accumulate the data of wafers that recently have been processed on the same processing device as that of the current wafer. Such a method increases the statistical basis for establishing compensating adjustments.

While in the first aspect, the quality measurements of the wafer are used directly to adjust the processing parameters of the same wafer, the second aspect considers a situation, where this is not possible. In case the metrology tool performs the measurement after the wafer has been processed, the measurement results can be fed back to the control unit of the processing tool, e. g. the lithography tool, which follows a CMP-step. The prerequisite according to this aspect therefore is that the knowledge of which compensation is necessary for which processing parameter for the adjustment has to be built up by the control unit priorily. This is provided by the feedback mechanism of the metrology results. A following semiconductor device, e. g. wafer, which has experience the same preceding processing device as the current semiconductor device, or wafer, essentially is adjusted by input from the current, or preceding, respecting, wafer measurement results. As in the previous aspect, data from just the pre-

ceding semiconductor device or accumulated data can be used to adjust the processing parameters of wafers, all having experienced the same preceding processing device.

In a further aspect, the control unit is considered to calculate the new set of values for adjusting the processing parameters combining the metrology measurement results and the token of a semiconductor wafer. In a preferable embodiment, a database matrix is set up in which for each processing device the resulting quality measurement results are noticed, and from which by setting up a system of rules or formulas, a conversion from measurement results into processing parameter adjustments or compensations can be calculated. Each new semiconductor device quality measurement is attached to this database matrix for both aspects of feed-forward or feed-back methods.

According to one aspect, simple fuzzy logic rules can be set up to hold the system and do the calculation a straight forward as possible and allow an improvement of the rules on a day-to-day basis. If e. g. it is found that substantially one processing parameter is related to one substantially one metrology parameter, i.e. measurement parameter, engineers may adapt the relation according to the most recent results or findings.

In another aspect, a more sophisticated relationship between measurement results and processing parameters can be set up by establishing a neural network. The control unit then comprises an essentially self-learning system that is improved with each new quality measurement input.

The database, or database matrix, at least needs the information of the individual semiconductor device identification, the processing device number, and the adjusted values of the set of processing parameters, or alternatively the measurement results prior to being converted to adjusted values. In

a further aspect, the semiconductor devices, in particular semiconductor wafers, are considered to be structured with minimum feature sizes of less than 0.14 µm. For these products, the statistical scatter measured in metrology tools have become particularly important. Therefore, the present method particularly improves the yield when manufacturing these products.

In a further aspect, the processing devices used in the preceding step are considered to be processing tools, e. g. CMP-apparatus, lithography tools, etc. or are considered to be processing chambers of one or more of the processing tools, since also chamber-to-chamber variations have been observed by the inventors, or processing heads for holding a semiconductor device in a processing tool like CMP-heads, etching wafer chucks, hot or cool plates, coater chucks, etc. Also for the latter devices, head-to-head variations resulting in differing metrology parameters have been observed and can advantageously according to the present invention be compensated by adjusting the processing parameters of each wafer individually.

Further aspects and advantages are evident from the dependent claims.

The invention will be better understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings, wherein

figure 1 shows a method for adjusting processing parameters according to prior art,

figure 2 shows an embodiment of the present invention for adjusting processing parameters in a lithographic tool by feeding back metrology measurement results,

figure 3 shows an embodiment according to the present invention for adjusting the processing parameters of an etching tool by feeding forward metrology measurement results.

The method of adjusting processing parameters of a lithographic tool as an example of prior art is shown in figure 1. A section of a sequence of processing steps for manufacturing a semiconductor wafer schematically comprises a group of CMP-apparatus 2a, 2b followed by the lithographic tool 1, which is followed by an overlay tool 3. Lithography tool 1 is controlled by a control unit 5 to which attached is a database 6.

A lot of semiconductor wafers 20 is input to the CMP-apparatus 2a, 2b for processing. The lot of wafers is combined into a semiconductor wafer carrier. After polishing semiconductor wafers 20 are loaded back into the device carrier and transferred to the lithography tool 1. From precedingly processed wafer lots, the control unit 5 gained information, which is stored in database 6, how to adjust the lithography parameters exposure dose, focus channel and alignment parameters in order to retrieve the highest lithography step yield with respect to critical dimension and overlay specification. Implicitly, the control unit compensates for an average offset of all CMP-apparatus present and actively processing in the fab.

After carrying out the lithography step, the wafers are transferred to the overlay tool 3 performing the critical dimension and overlay measurement. If the wafers 20 pass the metrology examination, they are moved forward for further processing. If the wafers 20 failed to lie within specifications, they are moved into rework into lithography tool 1. The corresponding measurement results in any case are sent to the control unit in order to improve the databases on which an adjustment is decided.

In order to try out a reasonable guess for the processing parameters, test wafers 21 are added and processed first in lithography tool 1. In overlay tool 3 they are then examined in order to verify the correctness of the process parameter guess. Eventually, the guess that was successful and the whole lot of wafers 20 is processed with these parameters irrespective of the CMP-apparatus used before. Probably, some wafers 20 still fail to pass the overlay control. The success of the current set of processing parameters is noted to control unit 5.

A first embodiment according to the method of the present invention revealing the aspect of feeding back metrology measurements is shown in figure 2. The same sequence of processing steps and devices as shown in figure 1 are displayed.

After being processed in CMP-apparatus 2a, 2b, the semiconductor wafers 20 of a lot are associated with a token 10a, 10b each, generated and performed by the fabrication-wide CIM-system. The token is a data string containing the lot number, the slot number in the wafer carrier, and the processing device number. If occasionally wafers 20 are unloaded and loaded to a new carrier, a possible new slot number for a wafer is tracked and the token is updated. The token is then submitted to the control unit 5 of the lithography tool 1. A database 6 is made available to the control unit 5 comprising information, i. e. a database matrix, of what compensation in terms of lithography parameter adjustment is necessary for a wafer 20 depending on which processing device 2a, 2b has been used to polish said wafer 20.

Eventually, the wafers 20 subsequently are introduced to the lithography tool 1, and by unloading the wafers 20 from the carrier, the control unit retrieves the wafer identification, i. e. the lot number and the slot number. The control unit 5 evaluates the corresponding token, which also has been stored

in a database table, and thereby retrieves the CMP-apparatus used by this wafer. The control unit 5 then adjusts the lithography tool parameter settings of alignment, exposure dose, and focus channel in order to compensate for the individual CMP-tool-offsets or variations.

After the lithography step, the semiconductor wafers 20 are transferred to the overlay tool 3, which performs the overlay and critical dimension measurement. Due to the compensation improvement, re-work is strongly reduced and is contributed to unexpected events. These will be communicated to the control unit 5 and the database node. This may result in an additional correction with a requirement for engineering analysis of result, or an action notification sent to an engineer requiring an action or a disposition.

According to figure 2, the overlay measurement is considered to be successful and the metrology measurement results are fed back to control unit 5 to be stored in database 6. There, with the help of neuronal network, a suitable relation is formed, and improved between compensational adjustment and metrology measurement result. This relation can be established since the tokens 10a, 10b remained active and were still known to overlay tool 3. The newly calculated CMP-apparatus dependent exposure parameter settings are then used for the next wafer lot as input in lithography tool 1.

Another embodiment according to the method of the present invention revealing the feed-forward mechanism is shown in figure 3. Semiconductor wafers 20 are introduced to a deposition process in CVD-tools 2a, 2b. The sequence is followed by a thickness measurement step in ellipsometer 3 and - among other lithography steps - a developing step in lithography clusters 2a', 2b' being a combination of exposure tool and photoresist track. This is followed by a metrology step in overlay tool 3'. In an etching step, the processing parameters of a processing tool 1, i. e. etching tool, are to be

adjusted for each wafer, to compensate for variations from CVD-tool to CVD-tool and from developer cup to developer cup.

The lot is split onto a group of CVD-tools 2a, 2b, and each wafer is supplied with tokens 10a, 10b, generated by the fab-wide CIM-system.

The thickness measurement results performed by ellipsometer 3 are forwarded to control unit 5, each result being connected to a wafer identification. Control unit 5 stores the results in a database matrix 6.

Meanwhile, semiconductor wafers 20 have entered a group of lithographic clusters 2a', 2b' being split to be manufactured in parallel.

After being developed, each in one of the developer cups within the lithography clusters 2a', 2b', the processing device numbers corresponding to the lithography clusters, or developer cups, are added to the first tokens 10a, 10b to give increased tokens 10a', 10b', 10a'', 10b''. The tokens now comprise the wafer identification, the CVD-apparatus number, and the developer cup number. The wafer identification consists of the lot number or the carrier number, and the slot number in which the corresponding wafer resides.

A critical dimension measurement in overlay tool 3' is then performed and the measurement results are submitted to the control unit 5. Eventually, semiconductor wafers 20 are introduced to the etching tool 1.

The database 6 now comprises the following table:

Wafer:	1	2	3	4	...	25
CVD cham-	A	b	A	B	...	B

ber:						
devel-oper cup:	1	1	2	1	...	2
etch tool:	X	X	X	X	X	X

The CVD-chambers employed here are named "A", "B", and the developer cups are numbered "1", "2". There is just one etching tool named "X".

The CVD-chamber and the developer cup have daily checks performed to give default values of all devices. Tool-offset values reflecting the compensation necessary to perform, are then:

A = thickness daily check + 5 nm
B = thickness daily check - 2 nm
1 = CD daily check + 9 nm
2 = CD daily check + 3 nm.

The process parameter to be determined and adjusted in the etching tool 1 is the etch time. A rule is set up with

$$X = f(\text{CVD-chamber, developer cup}).$$

The function f is periodically improved by fuzzy logic. For each wafer introduced to the etching tool 1, the wafer identification, i. e. slot number and lot number, are read out by the control unit 5 and the database entries in the above table are then used in combination with the formula for the etch time to adjust the etch time for each wafer individually. Since all quality measurement results are fed to the control unit 5 forwardly, even individual wafer effects in said processing devices can be compensated by the adjustment.

The yield is advantageously improved and the quality enhanced.

List of reference numerals:

1	processing tool, lithographic tool
2, 2a, 2b	processing device, performing preceding step
3	metrology tool
5	control unit
6	database
10a, 10b	token
20	plate-like object, semiconductor device or wafer
21	test wafers, test plate-like objects

Claims:

1. Method for adjusting processing parameters of at least one plate-like object (20) in a processing tool (1), said plate-like object (20) being to experience at least one preceding processing step performed each by one processing device (2a) out of at least one set of processing devices (2a, 2b), the adjustment in said processing tool (1) being controlled by a control unit (3), comprising the steps of

- providing a plate-like object (20) to said processing device (2a),
- processing said plate-like object (20),
- generating a token (10a) associated with said plate-like object (20), representing the processing device (2a) that has been used for the preceding processing step,
- transferring said token (10a) to said control unit (5),
- transferring said plate-like object (20) to said processing tool (1),
- adjusting the process parameters of said processing tool (1) using said control unit (5) in dependence of said token (10a),
- performing the process step on said plate-like object (20) in said processing tool (1) using the adjusted process parameters.

2. Method according to claim 1,
c h a r a c t e r i z e d i n that
a first plate-like object (20) associated with a first token (10a) is adjusted with a first set of values for process parameters and a second plate-like object (20') associated with a second token (10b) is adjusted with a second set of values for process parameters, said second set of values being different from said first set of values.

3. Method according to anyone of claims 1 or 2,
c h a r a c t e r i z e d i n that

said processing device (20) is a semiconductor wafer, said processing tool (1) is a lithographic tool, and the preceding processing step is at least one of the following:
- chemical mechanical polishing,
- etching,
- chemical vapor deposition,
- diffusion,
- wet processing,
- thin film deposition.

4. Method according to anyone of claims 1 or 2,
c h a r a c t e r i z e d b y
- transferring said at least one plate-like object (20) to a metrology tool (3) after having performed the at least one preceding processing step in a processing device (2a),
- performing at least one of a critical dimension measurement or overlay measurement,
- forwarding the metrology results of said measurement to the control unit (5).

5. Method according to anyone of claims 1 to 3,
c h a r a c t e r i z e d b y
- transferring said at least one semiconductor wafer to a metrology tool (3) after having performed the lithographic processing step,
- performing at least one of a critical dimension measurement or overlay measurement,
- transferring the metrology results of said measurement back to the control unit (5).

6. Method according to anyone of claims 4 or 5,
c h a r a c t e r i z e d i n that
said control unit (5) calculates a new set of values for adjusting the process parameters as a result of said metrology measurement and said token (10a).

7. Method according to claim 6,
c h a r a c t e r i z e d i n that
said calculation is performed by use of fuzzy logic rules.

8. Method according to claim 6,
c h a r a c t e r i z e d i n that
said calculation is performed by use of a neuronal network.

9. Method according to anyone of claims 6 to 8,
c h a r a c t e r i z e d i n that
said control unit (5)
- stores the new set of adjusted process parameters as an entry in a database, which comprises for each plate-like object (20) at least the individual plate-like object identification, the processing device number, and the adjusted values of the set of process parameters,
- performs said calculation from information stored in said database.

10. Method according to anyone of claims 3 or 5 to 10,
c h a r a c t e r i z e d i n that
the process parameters to be adjusted for a semiconductor wafer precedingly processed in a processing device (2a) are at least one of exposure dose, alignment settings, or focus channels of a lithographic tool (1).

11. Method according to claims 1 to 11,
c h a r a c t e r i z e d i n that
the patterns structured on the surface layers of said plate-like object (20) have a minimum resolution width of less than 0.25 μm.

12. Method according to claims 1 to 11,
c h a r a c t e r i z e d i n that
said processing devices (2a, 2b) are either one of processing tools, or processing chambers of a processing tool, or proc-

essing heads for holding a plate-like object (20) in a processing tool.

Abstract:

Method for adjusting processing parameters of at least one plate-like object in a processing tool

Processing parameters of at least one plate-like object(20), e.g. a semiconductor device or wafer, or a flat panel display, in a processing tool (1) are adjusted depending on which processing device (2a) out of at least one set of processing devices (2a, 2b) has been used for the semiconductor device (20) in a preceding step. This is provided by generating a virtual or physical token (10a), which connects the semiconductor device (20) identification with the processing device (2a, 2b) identification. This enables a compensation of tool-dependent effects in previous processing of a single device. An example is chemical mechanical polishing prior to lithography, where alignment marks can be deteriorated differently between CMP-apparatus. The amount of compensation is detected and evaluated by means of metrology tools, which - depending on the sequence of the metrology step relative to the processing step to be adjusted - either feed-forward or feed-backward their results to the processing tool (1). The yield of semiconductor device production is advantageously increased.

Figure 2

Fig. 1 (prior Art) 1/3

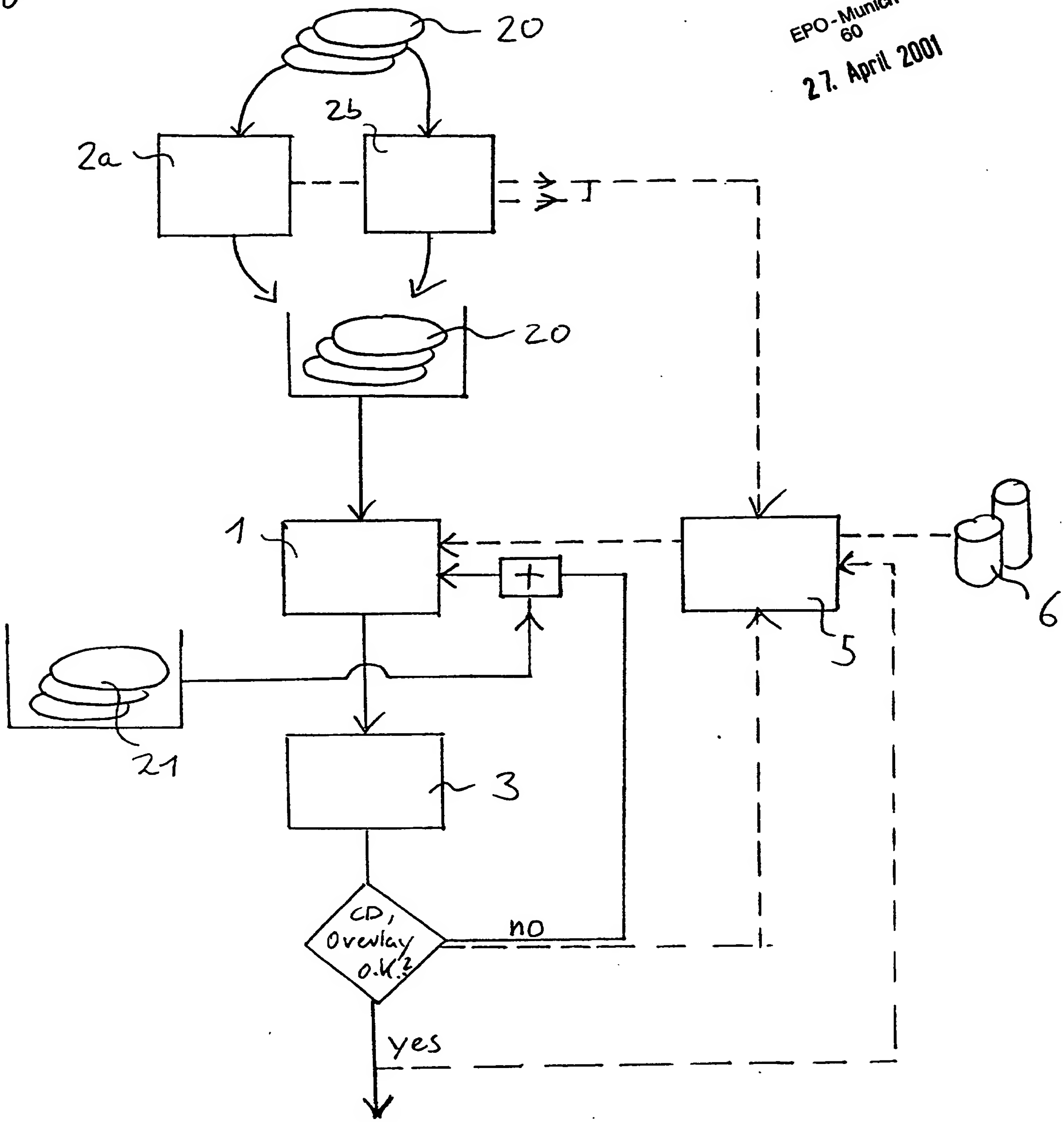

Fig 2

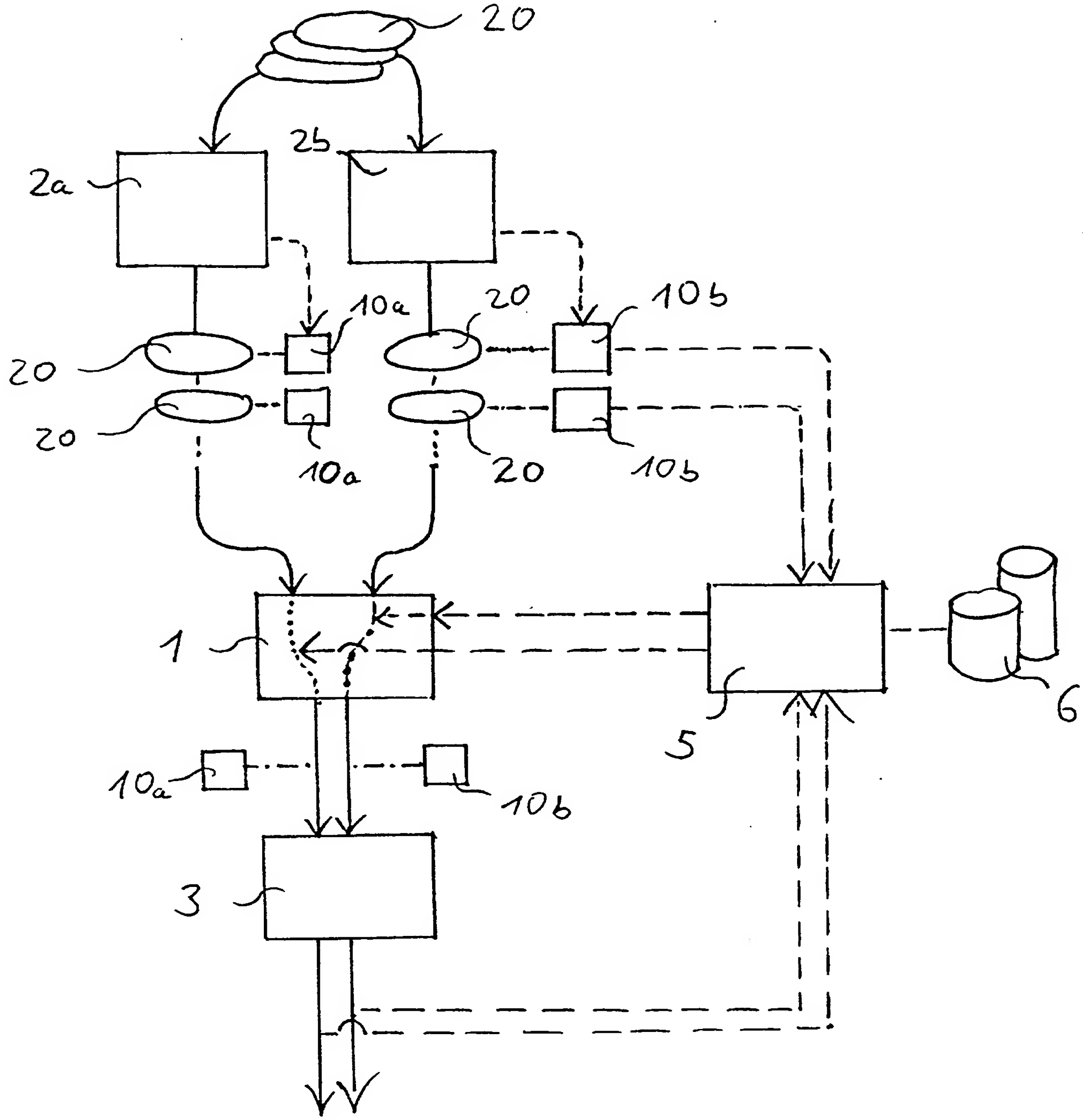

Fig. 3